CCS Technical Documentation
NAM-2 Series Transceivers

System Module DF9

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Transceiver NAM–2

Introduction

The NAM–2 is a dual band transceiver unit designed for the GSM900 (including EGSM) and GSM1800 networks. It is both GSM900 phase 2 power class 4 transceiver (2W) and GSM1800 power class 1 (1W) transceiver.

The transceiver consists of System/RF module, Display module and assembly parts.

The transceiver has a full graphic display and the user interface is based on a Jack style UI with two soft keys.

A back mounted antenna is used, there is no connection to an external antenna.

The transceiver has a low leakage tolerant earpiece and an omnidirectional microphone located in the mainframe, providing an excellent audio quality. The transceiver supports a full rate, an enhanced full rate and a half rate speech decoding feature.

The small SIM (Subscriber Identity Module) card is located below the back cover of the phone.

Operation Modes

There are five different operation modes:

- power off mode
- idle mode
- active mode
- charge mode
- local mode

In the power off mode only the circuits needed for power up are supplied.

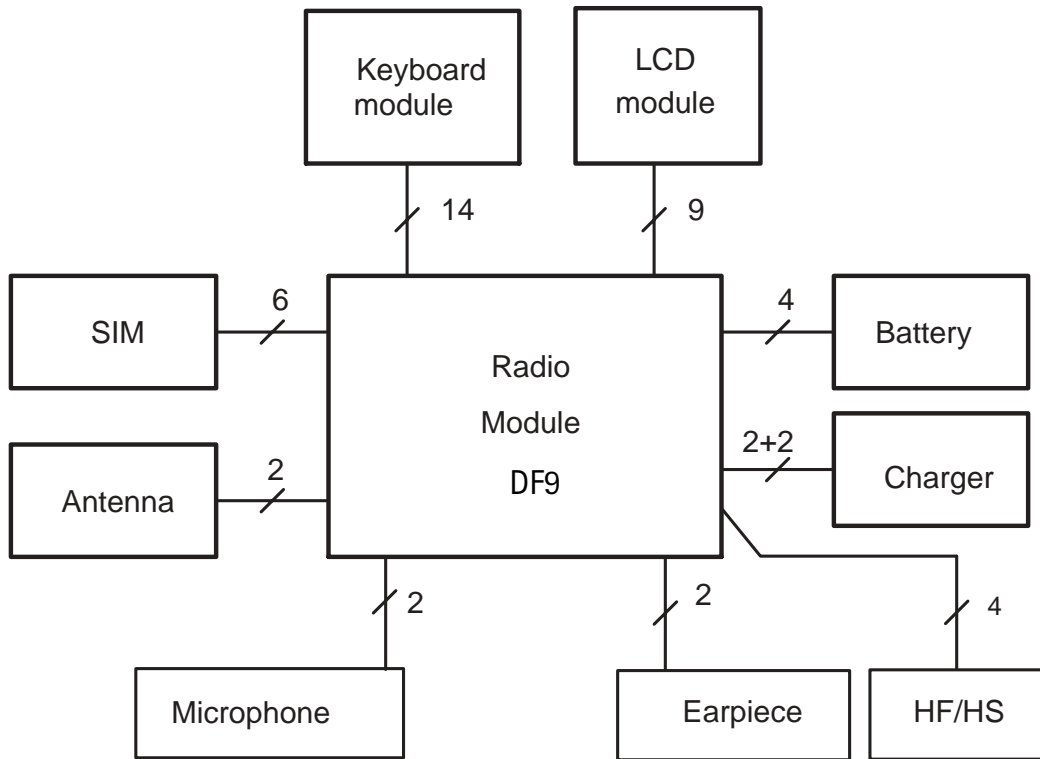In the idle mode circuits are powered down and only sleep clock is running.

In the active mode all the circuits are supplied with power although some parts might be in the idle state part of the time.

The charge mode is effective in parallel with all previous modes. The charge mode itself consists of two different states, i.e. the fast charge and the maintenance mode.

The local mode is used for alignment and testing.

Interconnection Diagram

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┌──────────────┐      ┌──────────────┐
│  Keyboard    │      │    LCD       │
│  module      │      │  module      │
└──────┬───────┘      └──────┬───────┘
      14                     9

┌──────────┐  6  ┌─────────────────┐  4  ┌──────────────┐
│   SIM    │─────│                 │─────│   Battery    │
└──────────┘     │     Radio       │     └──────────────┘
                 │                 │
                 │     Module      │  2+2┌──────────────┐
┌──────────┐  2  │                 │─────│   Charger    │
│ Antenna  │─────│     DF9         │     └──────────────┘
└──────────┘     └──┬──────┬───────┘
               2    │    2 │       4
        ┌──────────┐  ┌──────────┐  ┌──────────┐
        │Microphone│  │ Earpiece │  │  HF/HS   │
        └──────────┘  └──────────┘  └──────────┘
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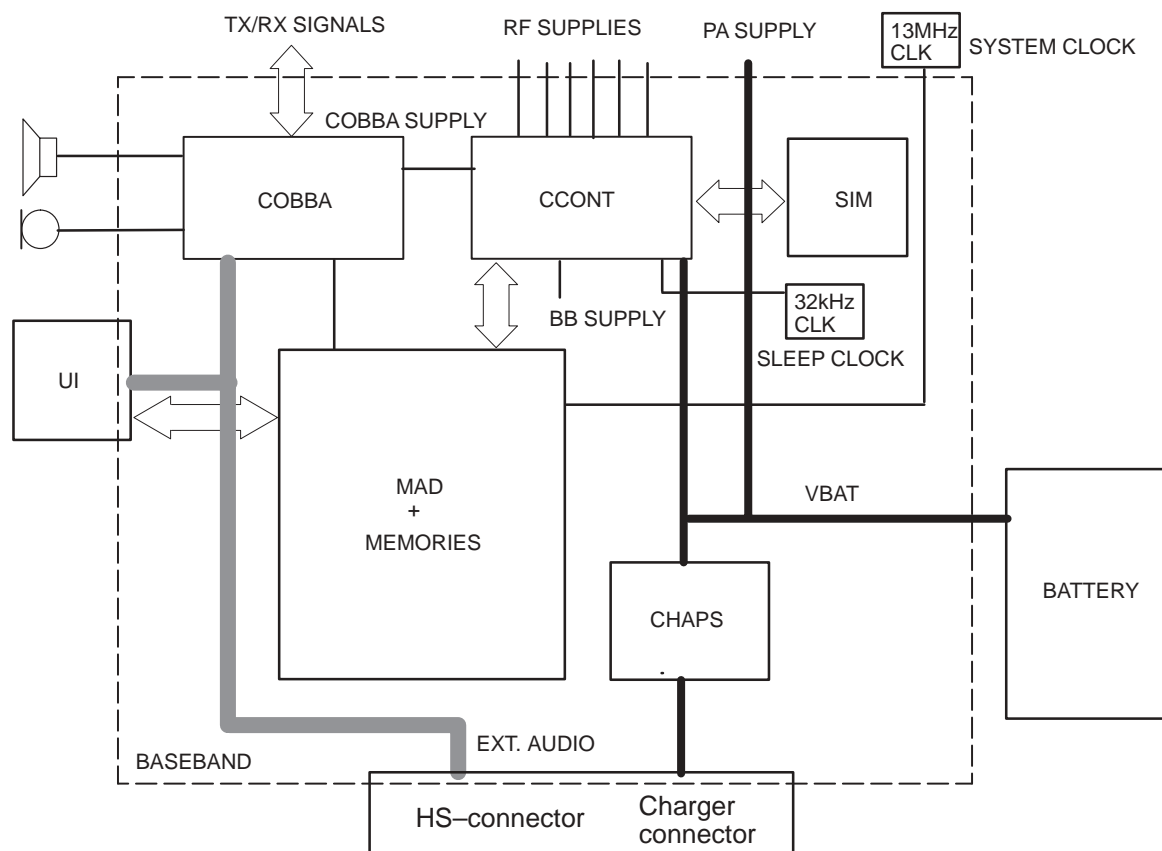
System Module

Baseband Module

The baseband architecture supports a power saving function called "sleep mode". This sleep mode shuts off the VCTCXO, which is used as system clock source for both RF and baseband. During the sleep mode the system runs from a 32 kHz crystal. The phone is waken up by a timer running from this 32 kHz clock supply. The sleeping time is determined by some network parameters. The sleep mode is entered when both the MCU and the DSP are in standby mode and the normal VCTCXO clock has been switched off.

The battery charging is controlled by a PWM signal from the CCONT. The PWM duty cycle is determined by a charging software and is fed to the CHAPS charging switch.

Standard chargers (two wires) provide coarse supply power, which is switched by the CHAPS for suitable charging voltage and current. Advanced chargers (three wires) are equipped with a control input. Three wire chargers are treated like two wire ones.

Block Diagram

Technical Summary

The baseband module consists four ASICs; CHAPS, CCONT, COBBA-GJP and MAD2WD1, which take care of the baseband functions of the engine.

The baseband is running from a 2.8V power rail, which is supplied by a power controlling ASIC CCONT. In the CCONT there are 6 individually controlled regulator outputs for RF-section and two outputs for the base band. In addition there is one +5V power supply output (V5V). The CCONT contains also a SIM interface, which supports both 3V and 5V SIM-cards.

The interface between the baseband and the RF section is mainly handled by a COBBA ASIC. COBBA provides A/D and D/A conversion of the in-phase and quadrature receive and transmit signal paths and also A/D and D/A conversions of received and transmitted audio signals to and from the user interface. The COBBA supplies the analog TXC and AFC signals to RF section according to the MAD DSP digital control. Data transmission between the COBBA and the MAD is implemented using se rial bus for high speed signalling and for PCM coded audio signals. Digital speech processing is handled by the MAD ASIC. COBBA is a dual volt age circuit, the digital parts are running from the baseband supply VBB and the analog parts are running from the analog supply VCOBBA.

The baseband supports both internal and external microphone inputs and speaker outputs. Input and output signal source selection and gain control is done by the COBBA according to control messages from the MAD. Keypad tones, DTMF, and other audio tones are generated and encoded by the MAD and transmitted to the COBBA for decoding. A buzzer and an external vibra alert control signals are generated by the MAD with separate PWM outputs.

EMC shielding is implemented using a metallized plastic frame. On the other side the engine is shielded with PWB grounding. Heat generated by the circuitry will be conducted out via the PWB ground planes.

External and Internal Signals and Connections

This section describes the external electrical connection and interface levels on the baseband. The electrical interface specifications are collected into tables that covers a connector or a defined interface.

DC (charger) connector

DC (charger) connector is physically integrated in the same component with the accessory interface connector. DC connector has both jack and contact pads for desk stand.

Service connector

Name	Parameter	Min	Typ	Max	Unit	Remark
MBUS	Serial clock from the Prommer	0 2.0	logic low logic low	0.8 2.85	V	Prommer detection and Serial Clock for synchronous communication
FBUS_RX	Serial data from the Prommer	0 2.0	logic low logic high	0.8 2.85	V	Receive Data from Prommer to Baseband
FBUS_TX	Data ac knowledge to the Prommer	0 2.0	logic low logic high	0.5 2.85	V	Transmit Data from Base band to Prommer
GND	GND	0		0	V	Ground

The service connector is used as a flash programming interface for up dating (i.e. re-programming) the flash program memory and an electrical access for services to the engine.

When the flash prommer is connected to the phone supply power is provided through the battery contacts and the phone is powered up with a pulse given to the BTEMP line**.**

Battery connector

The BSI contact on the battery connector is used to detect when the battery is to be removed to be able to shut down the operations of the SIM card before the power is lost if the battery is removed with power on. The BSI contact disconnects earlier than the supply power contacts to give enough time for the SIM and LCD shut down.

Name	Min	Typ	Max	Unit	Notes
VBATT	3.0	3.9	4.2	V	Battery voltage
BSI	0		2.85	V	Battery size indication Phone has 100kohm pull up resistor. SIM Card removal detection (Treshold is 2.4V@VBB=2.8V)
	67	68	69	kohm	Battery indication resistor (BLd-3)
		22		kohm	Battery indication resistor (service battery)
BTEMP	0		1.4	V	Battery temperature indication Phone has a 100k (+-5%) pull-up resistor, Battery package has a NTC pull-down resistor: 47k+-5%@+25C, B=4000+-3%
	2.15	10	3 20	V ms	Phone power up by battery (input) Power up pulse width
	1.9 90	100	2.85 200	V ms	Battery power up by phone (output) Power up pulse width
	0		1	kohm	Local mode initialization (in production)
BGND	0		0	V	Battery ground

SIM card connector

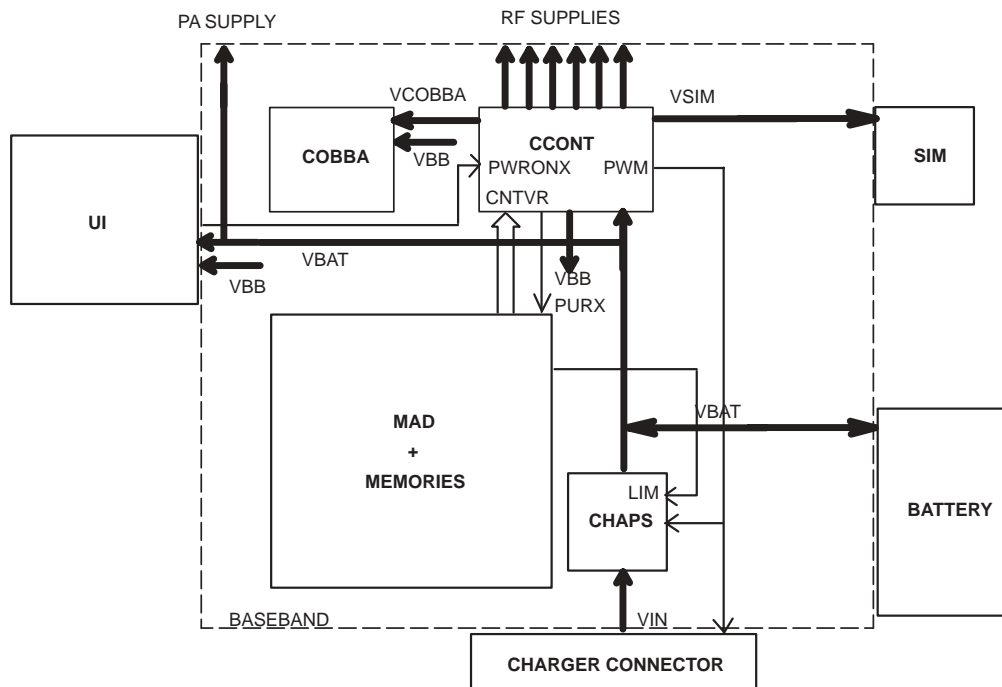The SIM card connector is located on the engine board beside the battery pack.

Pin	Name	Parameter	Min	Typ	Max	Unit	Notes
4	GND	GND	0		0	V	Ground
3, 5	VSIM	5V SIM Card 3V SIM Card	4.8 2.8	5.0 3.0	5.2 3.2	V	Supply voltage
6	DATA	5V Vin/Vout 3V Vin/Vout	4.0 0 2.8 0	"1" "0" "1" "0"	VSIM 0.5 VSIM 0.5	V	SIM data Trise/Tfall max 1us
2	SIMRST	5V SIM Card 3V SIM Card	4.0 2.8	"1" "1"	VSIM VSIM	V	SIM reset
1	SIMCLK	Frequency Trise/Tfall		3.25	25	MHz as	SIM clock

Power Distribution

In normal operation the baseband is powered from the phone`s battery. The battery consists of one Lithium-Ion cell. An external charger can be used for recharging the battery and supplying power to the phone.

The baseband contains parts that control power distribution to whole phone excluding those parts that use continuous battery supply. The battery feeds power directly to the CCONT and UI (buzzer and display and keyboard lights).
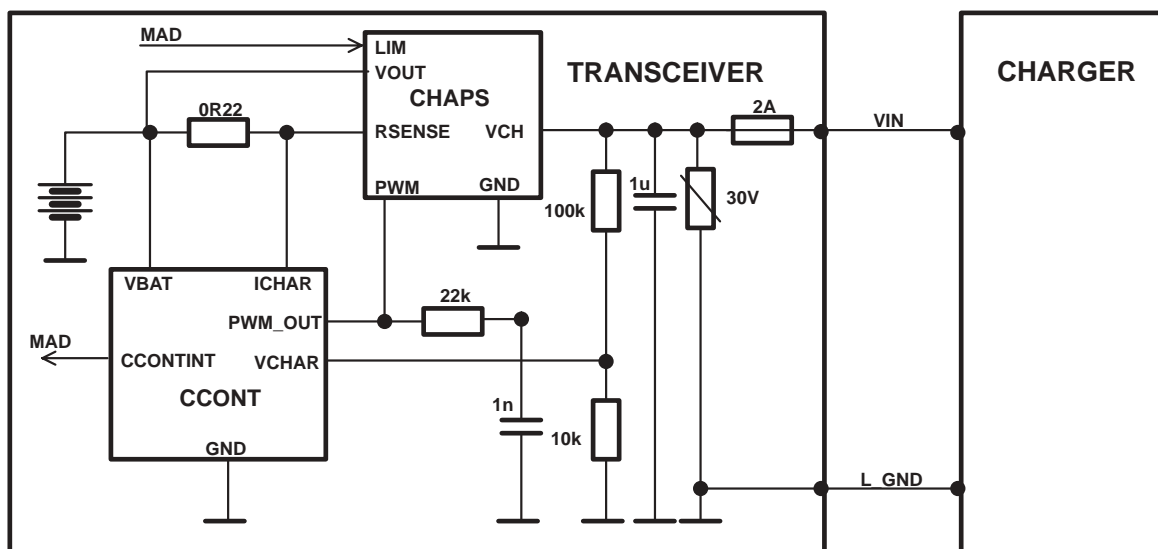
The power management circuit CHAPS provides protection against over voltages, charger failures and pirate chargers etc. that would otherwise cause damage to the phone.

Battery charging

The electrical specifications give the idle voltages produced by the acceptable chargers at the DC connector input. The absolute maximum in put voltage is 30V due to the transient suppressor that is protecting the charger input. At phone end there is no difference between a plug-in charger or a desktop charger. The DC-jack pins and bottom connector

charging pads are connected together inside the phone.

Startup Charging

When a charger is connected, the CHAPS is supplying a startup current minimum of 130mA to the phone. The startup current provides initial charging to a phone with an empty battery. Startup circuit charges the battery until the battery voltage level is reaches 3.0V (+/- 0.1V) and the CCONT releases the PURX reset signal and program execution starts. Charging mode is changed from startup charging to PWM charging that is controlled by the MCU software. If the battery voltage reaches 3.55V (3.75V maximum) before the program has taken control over the charging, the startup current is switched off. The startup current is switched on again when the battery voltage is sunken 100mV (nominal).

Parameter	Symbol	Min	Typ	Max	Unit
VOUT Start- up mode cutoff limit	Vstart	3.45	3.55	3.75	V
VOUT Start- up mode hysteresis NOTE: Cout = 4.7 uF	Vstarthys	80	100	200	mV
Start-up regulator output current VOUT = 0V... Vstart	Istart	130	165	200	mA

Battery Over voltage Protection

Output over voltage protection is used to protect phone from damage. This function is also used to define the protection cutoff voltage for different battery types (Li or Ni).
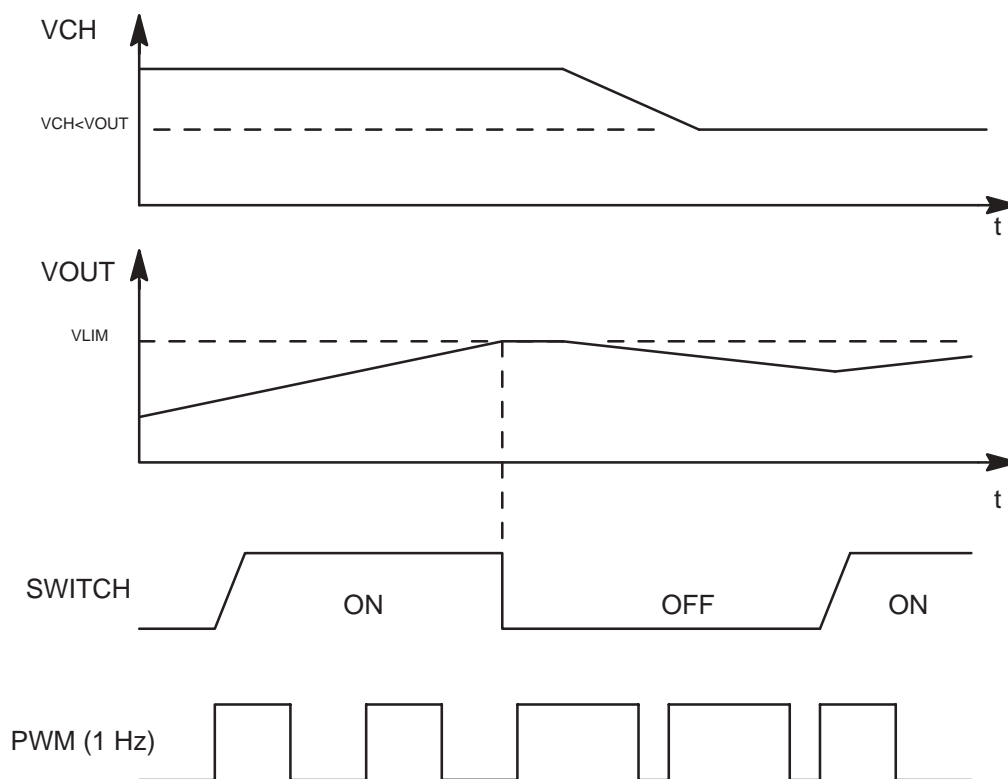
The power switch is immediately turned OFF if the voltage in VOUT rises above the

selected limit VLIM1 or VLIM2.

Parameter	Symbol	LIM input	Min	Typ	Max	Unit
Output voltage cutoff limit (during transmission or Li-battery)	VLIM	LOW	4.4	4.6	4.8	V

The voltage limit (VLIM1 or VLIM2) is selected by logic LOW or logic HIGH on the CHAPS (N101) VLIM input pin. In NAM-2 VLIM is fixed low in HW.

When the switch in output over voltage situation has once turned OFF, it stays OFF until the battery voltage falls below VLIM and PWM = LOW is detected. The switch can be turned on again by setting PWM = HIGH.
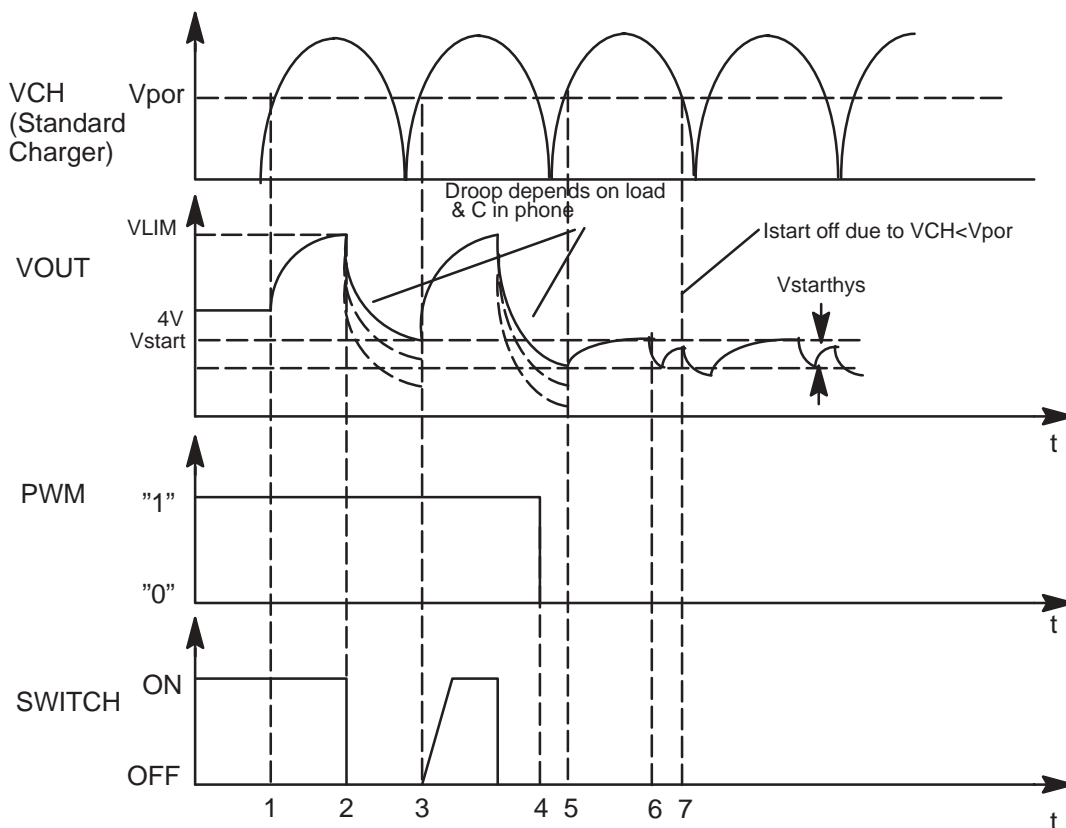

Battery Removal During Charging

Output over voltage protection is also needed in case the main battery is removed when charger connected or charger is connected before the battery is connected to the phone.

With a charger connected, if VOUT exceeds VLIM, CHAPS turns switch OFF until the charger input has sunken below Vpor (nominal 3.0V, maxi mum 3.4V). MCU software will stop the charging (turn off PWM) when it detects that battery has been removed. The CHAPS remains in protection state as long as PWM stays HIGH after the output over

voltage situation has occured.

1. Battery removed, (standard) charger connected, VOUT rises (follows charger voltage)
2. VOUT exceeds limit VLIM(X), switch is turned immediately OFF
3. VOUT falls (because no battery) , also VCH<Vpor (standard chargers full–rectified output). When VCH > Vpor and VOUT < VLIM(X) –> switch turned on again (also PWM is still HIGH) and VOUT again exceeds VLIM(X).
4. Software sets PWM = LOW –> CHAPS does not enter PWM mode
5. PWM low –> Startup mode, startup current flows until Vstart limit reached
6. VOUT exceeds limit Vstart, Istart is turned off
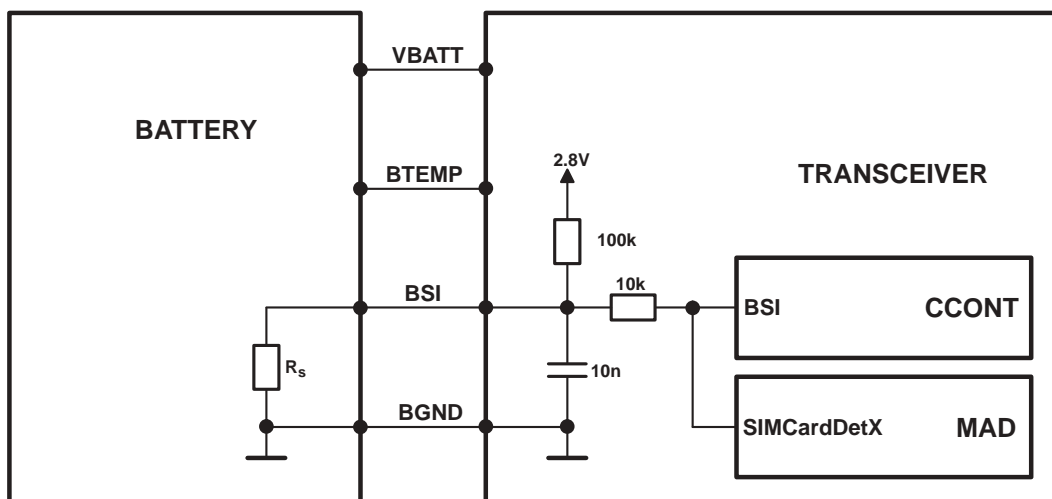7. VCH falls below Vpor

PWM

When a charger is used, the power switch is turned ON and OFF by the PWM input. PWM rate is 1Hz. When PWM is HIGH, the switch is ON and the output current Iout = charger current - CHAPS supply current. When PWM is LOW, the switch is OFF and the output current Iout = 0. To pre vent the switching transients inducing noise in audio circuitry of the phone soft switching is used.
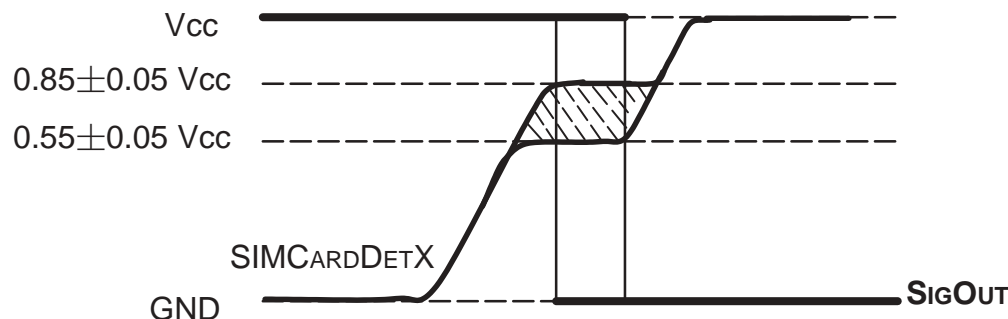
Battery Identification

Different battery types are identified by a pull-down resistor inside the battery pack. The BSI line inside transceiver has a 100k pull-up to VBB. The MCU can identify the battery by reading the BSI line DC-voltage level with a CCONT (N100) A/D-converter.

Battery identification table :

Name	Min	Typ	Max	Unit	Notes
BSI	0		2.8	V	Battery size indication 100k pull-up resistor to VBB in phone SIM Card removal detection (Treshold is 2.4V@VBB=2.8V)
	67.3	68	68.8	kohm	Indication of a BLD-3 battery (720 mAh Li-Ion)
		22		kohm	Indication resistor for a service battery

The battery identification line is used also for battery removal detection. The BSI line is connected to a SIMCardDetX line of MAD2. SIMCardDetX is a threshold detector with a nominal input switching level 0.85xVcc for a rising edge and 0.55xVcc for a falling edge. The battery removal detection is used as a trigger to power down the SIM card before the power is lost. The BSI contact in the battery contact disconnects before the other contacts so that there is a delay between battery removal detection and supply power off.
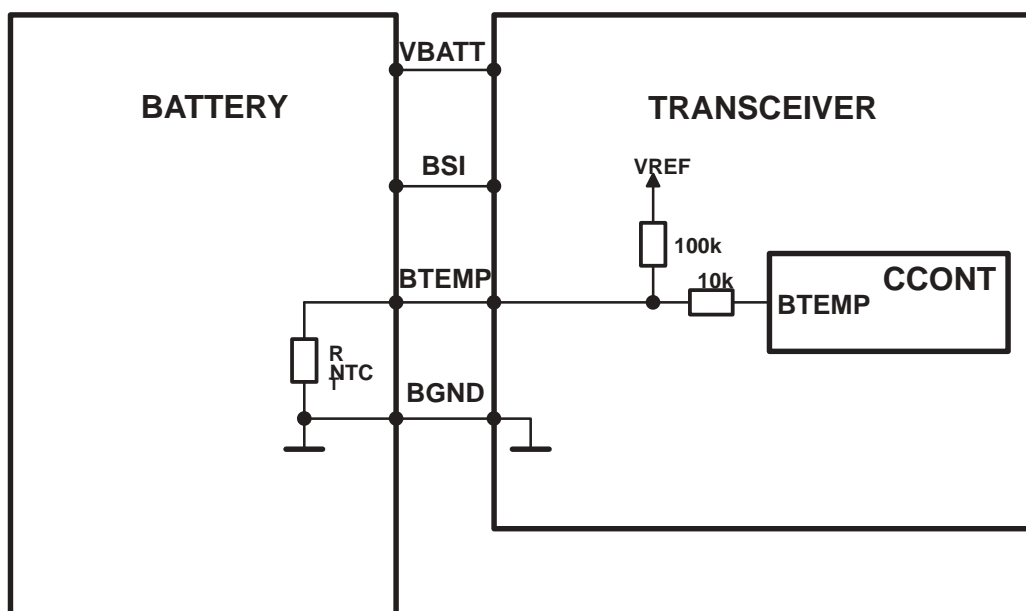

Battery Temperature

The battery temperature is measured with a NTC inside the battery pack. The BTEMP line

inside transceiver has a 100k pull-up to VREF. The MCU can calculate the battery temperature by reading the BTEMP line DC-voltage level with a CCONT (N100) A/D-converter.

Pin	Name	Min	Typ	Max	Unit	Notes
3	BTEMP	0		1.4	V	Battery temperature indication 100k pulpy resistor to VREF in phone Battery package has NTC pull down resistor: 47k +/-5%@+25C, B=4000+/-3%
		2.15	10	3 20	V ms	Phone power up by battery (input) Power up pulse width
		1.990	100	2.8 200	V ms	Battery power up by phone (output) Power up pulse width
		-5		5	%	100k pull-up resistor tolerance

Supply Voltage Regulators

The heart of the power distribution is the CCONT. It includes all the volt age regulators and feeds the power to the whole system. The baseband digital parts are powered from the VBB regulator which provides 2.8V baseband supply. The baseband regulator is active always when the phone is powered on. The VBB baseband regulator feeds MAD and memories, COBBA digital parts and the LCD driver in the UI section. There is a separate regulator for a SIM card. The regulator is selectable between 3V and 5V and controlled by the SIMPwr line from MAD to CCONT. The COBBA analog parts are powered from a dedicated 2.8V supply VCOB BA. The CCONT supplies also 5V for RF and for flash VPP. The battery is charged from the main battery voltage by the CHAPS when the main battery voltage is over 3.2V.

Operating mode	Vref	RF REG	VCOBBA	VBB	VSIM	SIMIF
Power off	Off	Off	Off	Off	Off	Pull down
Power on	On	On/Off	On	On	On	On/Off
Reset	On	Off VR1 On	On	On	Off	Pull down
Sleep	On	Off	Off	On	On	On/Off

Note: COBBA regulator is off in SLEEP mode. Its output pin may be fed from V_{BB} in SLEEP mode by setting bit RFReg(5) to '1' (default).

CCONT includes also five additional 2.8V regulators providing power to the RF section. These regulators can be controlled either by the direct control signals from MAD or by the RF regulator control register in CCONT which MAD can update. Below are the listed the MAD control lines and the regulators they are controlling.

- TxPwr controls **VTX regulator (VR5)**
- RxPwr controls **VRX regulator (VR2)**
- SynthPwr controls all the rf regulators except VR1
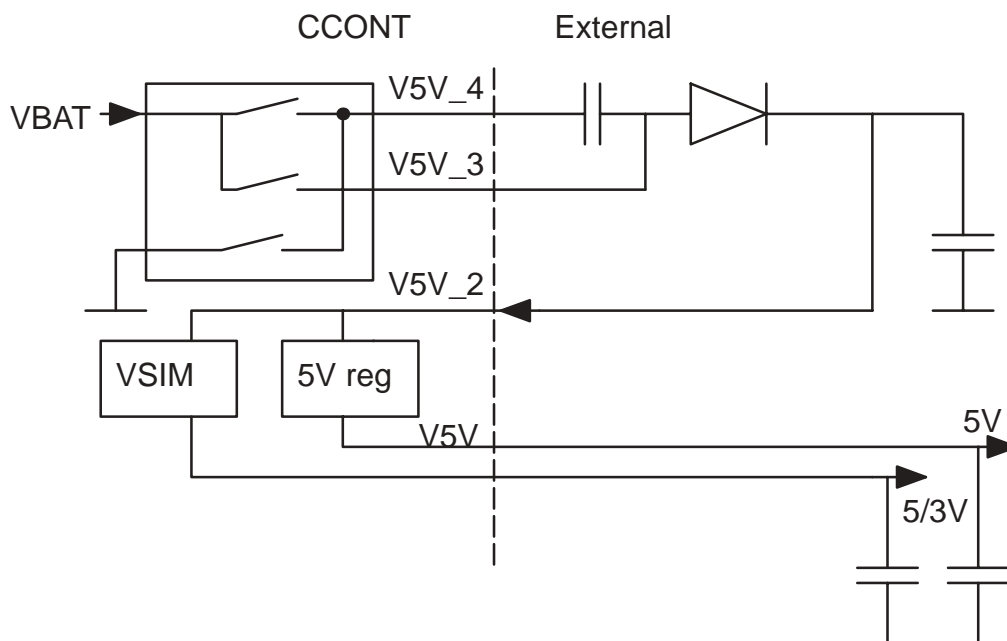- VCXOPwr controls VXO regulator (VR1)

In addition to the above mentioned signals MAD includes also TXP control signal which goes to HAGAR power control block. The transmitter power control TXC is led from COBBA to HAGAR.

Switched Mode Supply VSIM

There is a switched mode supply for SIM-interface. SIM voltage is selected via serial IO. The 5V SMR can be switched on independently of the SIM voltage selection, but can't be switched off when VSIM voltage value is set to 5V.

NOTE: VSIM and V5V can give together a total of 30mA.

In the next figure the principle of the SMR / VSIM-functions is shown.
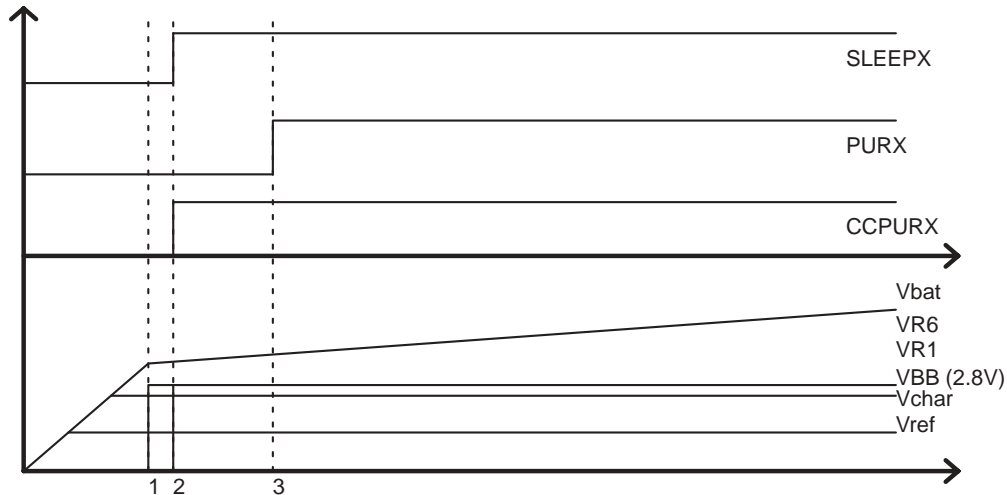

Power Up and Power Down

The baseband is powered up by:

1. Pressing the power key, that generates a PWRONX interrupt signal from the power key to the CCONT, which starts the power up procedure.

2. Connecting a charger to the phone. The CCONT recognizes the charger from the VCHAR voltage and starts the power up procedure.

3. A battery interrupt. Intelligent battery packs have a possibility to power up the phone. When the battery gives a short (10ms) voltage pulse through the BTEMP pin, the CCONT wakes up and starts the power on procedure.

Power up with a charger

When the charger is connected CCONT will switch on the CCONT digital voltage as soon as the battery voltage exceeds 3.0V. The reset for CCONT's digital parts is released when the operating voltage is stabilized (50 us from switching on the voltages). Operating voltage for VCXO is also switched on. The counter in CCONT digital section will keep MAD in reset for 62 ms (PURX) to make sure that the clock provided by VCXO is stable. After this delay MAD reset is released, and VCXO –control (SLEEPX) is given to MAD. The next diagram explains the power on procedure with charger (the picture assumes empty

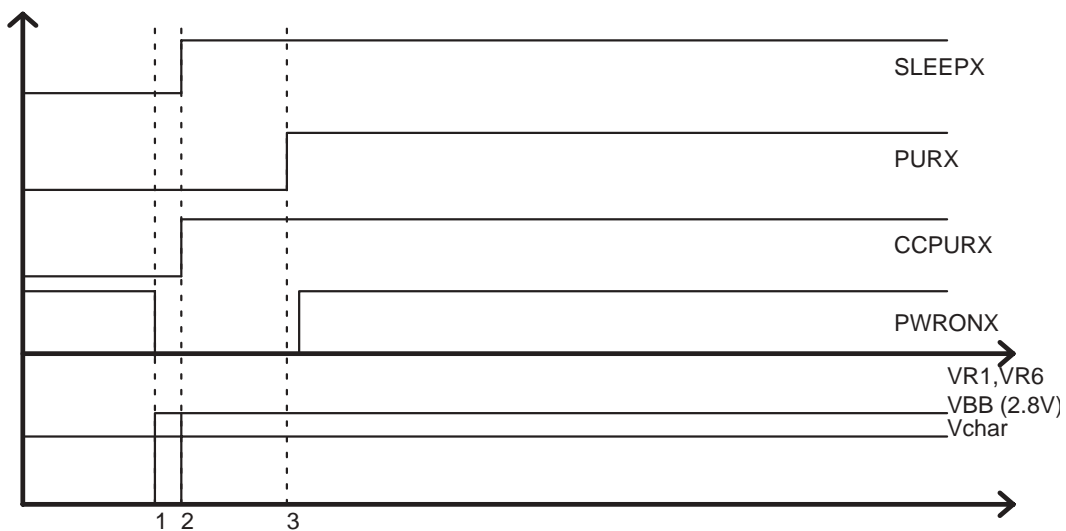battery, but the situation would be the same with full battery):

1: Battery voltage over 3.0==>Digital voltages to CCONT (VBB)
2: CCONT digital reset released. VCXO turned on
3: 62ms delay before PURX released

When the phone is powered up with an empty battery pack using the standard charger, the charger may not supply enough current for standard power-up procedure and the power-up must be delayed.

Power Up With The Power Switch (PWRONX)

When the power on switch is pressed the PWRONX signal will go low. CCONT will switch on the CCONT digital section and VCXO as was the case with the charger driven power up. If PWRONX is low when the 64 ms delay expires, PURX is released and SLEEPX control goes to MAD. If PWRONX is not low when 64 ms expires, PURX will not be released, and CCONT will go to power off (digital section will send power off signal to analog parts)

1:Power switch pressed ==> Digital voltages on in CCONT (VBB)
2: CCONT digital reset released. VCXO turned on
3: 62 ms delay to see if power switch is still pressed.

Power Up by IBI

IBI can power CCONT up by giving a short pulse (10ms) through the BTEMP line. After power-up BTEMP will act as any other input channel for ADC.

When the PURX reset is released, the MAD releases the system reset ExtSysResetX and the internal MCUResetX signals and starts the boot program execution from MAD bootrom if MAD GenSDIO pin is pulled low or from external memory if GenSDIO pin is pulled high. In normal operation the program execution continues from the flash program memory. If the MBUS line is pulled low during the power up the bootrom starts a flash programming sequence and waits for the prommer response through FBUS_RX line.

Power Down

The baseband is powered down by:

1.   Pressing the power key, that is monitored by the MAD, which starts the power down procedure.

2.   If the battery voltage is dropped below the operation limit, either by not charging it or by removing the battery.

3.   Letting the CCONT watchdog expire, which switches off all CCONT regulators and the phone is powered down.

The power down is controlled by the MAD. When the power key has been pressed long enough or the battery voltage is dropped below the limit the MCU initiates a power down procedure and disconnects the SIM power. Then the MCU outputs a system reset signal and resets the DSP. If there is no charger connected the MCU writes a short delay to CCONT watch dog and resets itself. After the set delay the CCONT watchdog expires, which activates the PURX and all regulators are switched off and the phone is powered down by the CCONT.

If a charger is connected when the power key is pressed the phone enters into the acting dead mode.

Modes of Operation

Acting Dead

If the phone is off when the charger is connected, the phone is powered on but enters a state called "acting dead". To the user the phone acts as if it was switched off. A battery charging alert is given and/or a battery charging indication on the display is shown to acknowledge the user that the battery is being charged.

Active Mode

In the active mode the phone is in normal operation, scanning for channels, listening to a base station, transmitting and processing information. All the CCONT regulators are operating. There are several substates in the active mode depending on if the phone is in burst reception, burst transmission, if DSP is working etc.

Sleep Mode

> In the sleep mode all the regulators except the baseband VBB and the SIM card VSIM regulators are off. Sleep mode is activated by the MAD after MCU and DSP clocks have been switched off. The voltage regulators for the RF section are switched off and the VCXO power control, VCXOPwr is set low. In this state only the 32 kHz sleep clock oscillator in CCONT is running. The flash memory power down input is connected to the Ext-SysResetX signal, and the flash is deep powered down during the sleep mode.

> The sleep mode is exited either by the expiration of a sleep clock counter in the MAD or by some external interrupt, generated by a charger connection, key press, headset connection etc. The MAD starts the wake up sequence and sets the VCXOPwr and ExtSysResetX control high. After VCXO settling time other regulators and clocks are enabled for active mode.

> If the battery pack is disconnect during the sleep mode, the CCONT pulls the SIM interface lines low as there is no time to wake up the MCU.

Charging

> Charging can be performed in any operating mode.The battery type/size is indicated by a resistor inside the battery pack. The resistor value corresponds to a specific battery capacity. This capacity value is related to the battery technology as different capacity values are achieved by using different battery technology.

> The battery voltage, temperature, size and current are measured by the CCONT controlled by the charging software running in the MAD.

> The power management circuitry controls the charging current delivered from the charger to the battery. Charging is controlled with a PWM input signal, generated by the CCONT. The PWM pulse width is controlled by the MAD and sent to the CCONT through a serial data bus. The battery voltage rise is limited by turning the CHAPS switch off when the battery voltage has reached 4.2 V. Charging current is monitored by measuring the voltage drop across a 220 mohm resistor.
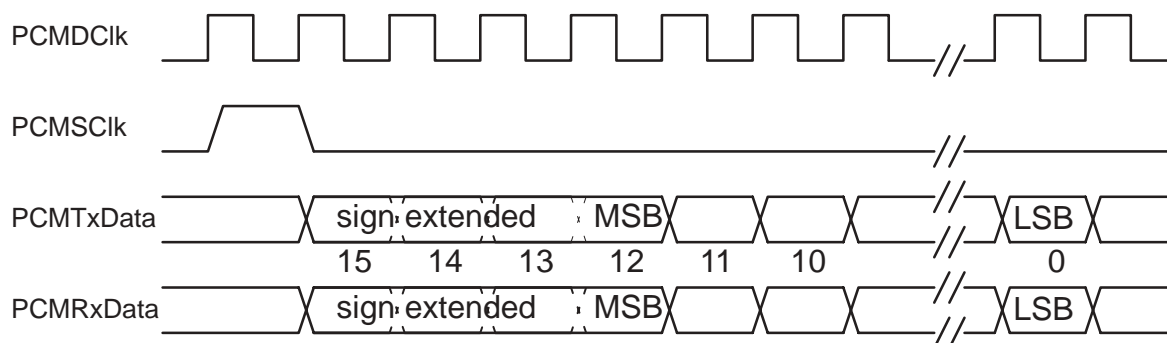
Watchdog

> The Watchdog block inside CCONT contains a watchdog counter and some additional logic which are used for controlling the power on and power off procedures of CCONT. Watchdog output is disabled when WDDisX pin is tied low. The WD-counter runs during that time, though. Watchdog counter is reset internally to 32 s at power up. Normally it is re set by MAD writing a control word to the WDReg.

Audio control

PCM serial interface

> The interface consists of following signals: a PCM codec master clock (PCMDClk), a frame synchronization signal to DSP (PCMSClk), a codec transmit data line (PCMTX) and a codec receive data line (PCMRX). The COBBA-GJP generates the PCMDClk clock, which is supplied to DSP SIO. The COBBA-GJP also generates the PCMSClk signal to DSP by dividing the PCMDClk. The PCMDClk frequency is 1.000 MHz and is generated by dividing

the RFIClk 13 MHz by 13. The COBBA-GJP further divides the PCMDClk by 125 to get a PCMSClk signal, 8.0 kHz.

Digital Control

The baseband functions are controlled by the MAD asic, which consists of a MCU, a system ASIC and a DSP.

MAD2 WD1

MAD2 WD1 contains following building blocks:

- ARM RISC processor with both 16-bit instruction set (THUMB mode) and 32-bit instruction set (ARM mode)

- TI Lead DSP core with peripherials:

- API (Arm Port Interface memory) for MCU-DSP communication, DSP code download, MCU interrupt handling vectors (in DSP RAM) and DSP booting.

- Serial port (connection to PCM)

- Timer

- DSP memory

- BUSC (BusController for controlling accesses from ARM to API, System Logic and MCU external memories, both 8- and 16-bit memories)

- System Logic

- CTSI (Clock, Timing, Sleep and Interrupt control)

- MCUIF (Interface to ARM via BᴜsC). Contains MCU Boo tROM

- DSPIF (Interface to DSP)

- MFI (Interface to COBBA AD/DA Converters)

- CODER (Block encoding/decoding and A51&A52 ciphering)

- AccIF (Accessory Interface)

- SCU (Synthesizer Control Unit for controlling 2 separate synthesizer)

- UIF (Keyboard interface, serial control interface for COBBA PCM Codec, LCD Driver and CCONT)

- SIMI (SimCard interface with enhanced features)

- PUP (Parallel IO, USART and PWM control unit for vibra and buzzer)

- Flexpool

The MAD2 operates from a 13 MHz system clock, which is generated from the 13Mhz VCXO frequency. The MAD2 supplies a 6,5 MHz or a 13 MHz internal clock for the MCU and system logic blocks and a 13 MHz clock for the DSP, where it is multiplied to 45.5 MHz DSP clock. The system clock can be stopped for a system sleep mode by disabling the VCXO supply power from the CCONT regulator output. The CCONT provides a 32 kHz sleep clock for internal use and to the MAD2, which is used for the sleep mode timing. The sleep clock is active when there is a battery voltage available i.e. always when the battery is connected.

The pins are not listed, being inaccessible for probing.

Memories

MAD memory configuration

The MAD2WD1 used in NAM–2 includes 16 kB RAM, and 80 kB ROM memory.

Memory

The MCU program code resides in an external flash program memory, the size of which is 16Mbits (1024k x 16bit). The MCU work (data) memory size comprises 2048 kbits (128k x 16bit). Flash and SRAM memory chips are packed in one combo memory package.

The BusController (BUSC) section in the MAD decodes the chip select signals for the external memory devices and the system logic. BUSC controls internal and external bus drivers and multiplexers connected to the MCU data bus. The MCU address space is divided into access areas with separate chip select signals. BUSC supports a programmable number of wait states for each memory range.

Program and Data Memory

The MCU program code resides in the program memory. The program memory is 16Mbits (1024k x 16bit) Flash memory.

The flash memory has a power down pin that should be kept low, during the power up phase of the flash to ensure that the device is powered up in the correct state, read only. The power down pin is utilized in the system sleep mode by connecting the ExtSysResetX to the flash power down pin to minimize the flash power consumption during the sleep.

Nonvolatile data memory is implemented with program (Flash) memory. Special EEPROM emulation (EEEMmu) software is utilized.

Work Memory

The work memory is a static RAM of size 2048k (128k x 16). The memory contents are lost when the baseband voltage is switched off. All retainable data must be stored into the data memory when the phone is powered down.

MCU Memory Requirements

Device	Organization	Access Time ns	Wait States Used	Remarks
FLASH	1024kx16	120	1	uBGA 48
SRAM	128kx16	120	1	uBGA 48

MCU Memory Map

MAD2 supports maximum of 4GB internal and 4MB external address space. External memories use address lines MCUAd0 to MCUAd21 and 8-bit/16-bit databus. The BUSC bus controller supports 8- and 16-bit access for byte, double byte, word and double word data. Access wait states (0, 1 or 2) and used databus width can be selected separately for each memory block.

Flash Programming

The phone have to be connected to the flash loading adapter so that sup ply voltage for the phone and data transmission lines can be supplied from/to the adapter. When adapter switches supply voltage to the phone, the program execution starts from the BOOT ROM and the MCU investigates in the early start-up sequence if the flash prommer is connected. This is done by checking the status of the MBUS-line. Normally this line is high but when the flash prommer is connected the line is forced low by the prommer.

The flash prommer serial data receive line is in receive mode waiting for an acknowledgement from the phone. The data transmit line from the baseband to the prommer is

initially high. When the baseband has recognized the flash prommer, the TX-line is pulled low. This acknowledgement is used to start to toggle MBUS (FCLK) line three times in order that MAD2 gets initialized. This must be happened within 15 ms after TX line is pulled low. After that the data transfer of the first two bytes from the flash prommer to the baseband on the RX-line must be done within 1 ms.

When MAD2 has received the secondary boot byte count information, it forces TX line high. Now, the secondary boot code must be sent to the phone within 10 ms per 16 bit word. If these time-out values are exceeded, the MCU (MAD2) starts normal code execution from flash. After this, the timing between the phone and the flash prommer is handled with dummy bites.

A 5V programming voltage is supplied inside the transceiver from the battery voltage with a switch mode regulator (5V/30mA) of the CCONT. The 5V is connected to VPP pin of the flash.

COBBA GJP

COBBA GJP ASIC provides an interface between the baseband and the RF-circuitry. COBBA performs analogue to digital conversion of the receive signal. For transmit path COBBA performs digital to analogue con version of the transmit amplifier power control ramp and the in-phase and quadrature signals. A slow speed digital to analogue converter will pro vide automatic frequency control (AFC).

COBBA is at any time connected to MAD asic with two interfaces, one for transferring TX and RX data between MAD and COBBA and one for transferring codec RX/TX samples.

RF Module

This RF module takes care of all RF functions of EGSM/DCS1800 dual band engine. RF circuitry is located on one side of the 8 layer transceiver-PWB. PWB area for the RF circuitry is about 15 cm2. The RF design is based on the first dualband direct conversion RF-IC "Hagar". So there is no intermediate frequency and that means the number of component is much lover than before and there shall be much less interference problems than previously.

EMC emissions are taken care of using metallized plastic shield, which screens the whole transceiver. Internal screening is realized with isolated partitions. At least the VCO is isolated. The baseband circuitry is located on the same side of the same board.
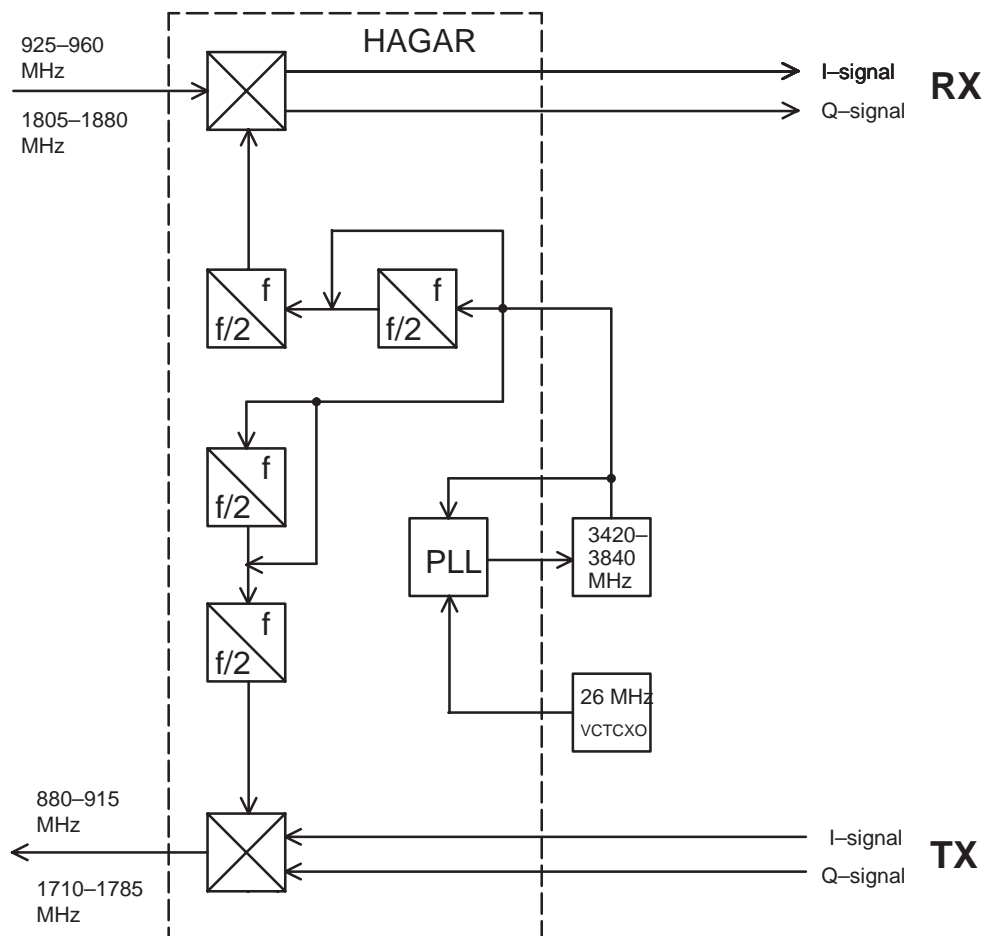
Maximum Ratings

Parameter	Rating
Battery voltage, idle mode	4.2 V
Regulated supply voltage	2.8 +/- 3% V
Voltage reference	1.5 +/- 1.5% V

Operating temperature range	–10...+55 deg. C
Absolute maximum battery voltage	4.8 V

RF Characteristics

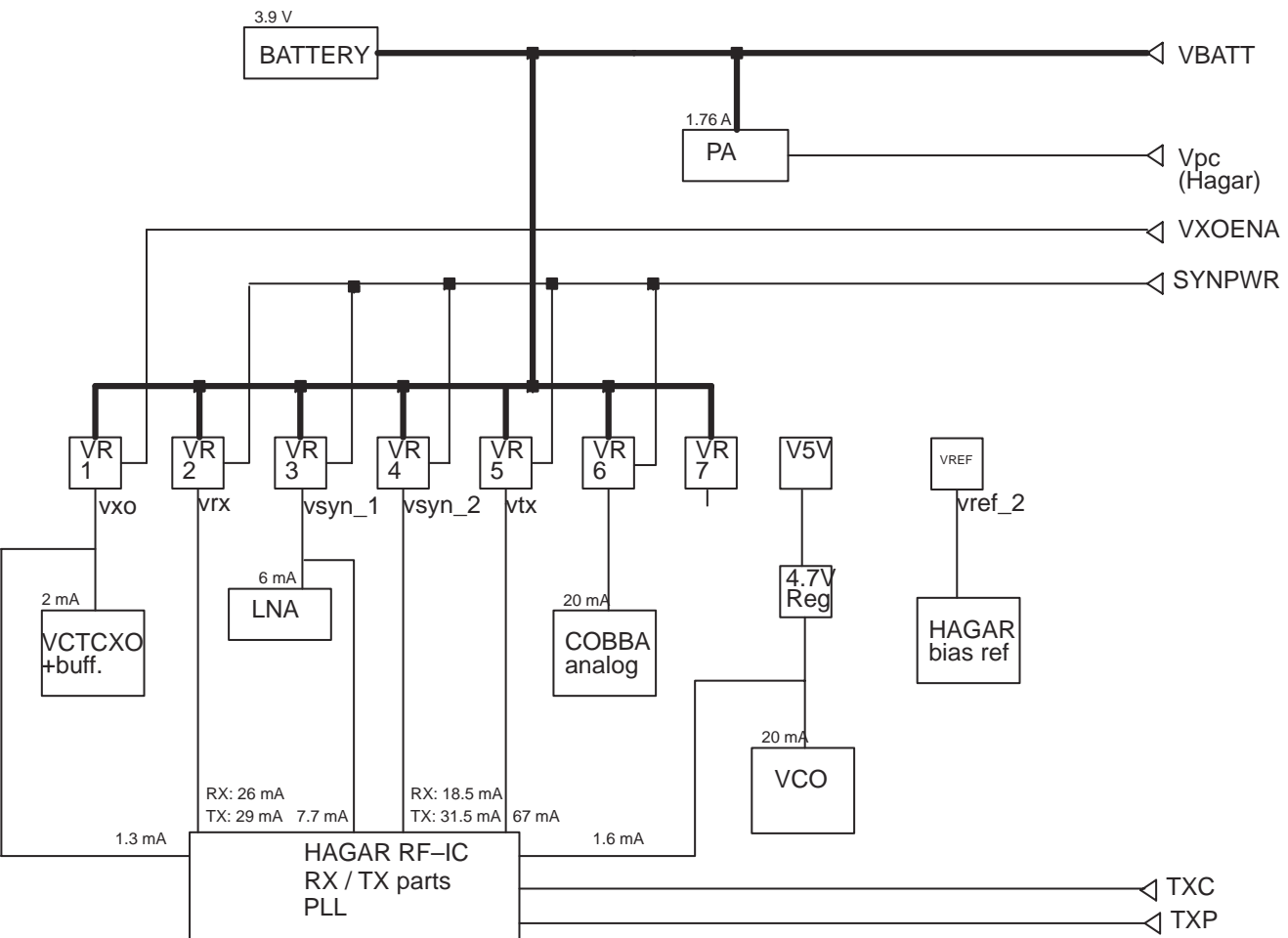| Item	Values (EGSM / DCS1800)
Receive frequency range	925... 960 MHz / 1805... 1880 MHz
Transmit frequency range	880... 915 MHz / 1710... 1785 MHz
Duplex spacing	45 MHz / 95 MHz
Channel spacing	200 kHz
Number of RF channels	174 / 374
Power class	4 (EGSM900) / 1 (DCS1800)
Number of power levels	15 / 16

RF Frequency Plan

DC characteristics

Regulators

> Transceiver has a multi function power management IC at baseband section, which contains among other functions, also 7 pcs of 2.8 V regulators. All regulators can be controlled individually with 2.8 V logic directly or through control register. In GSM direct controls are used to get fast switching, because regulators are used to enable RF-functions.
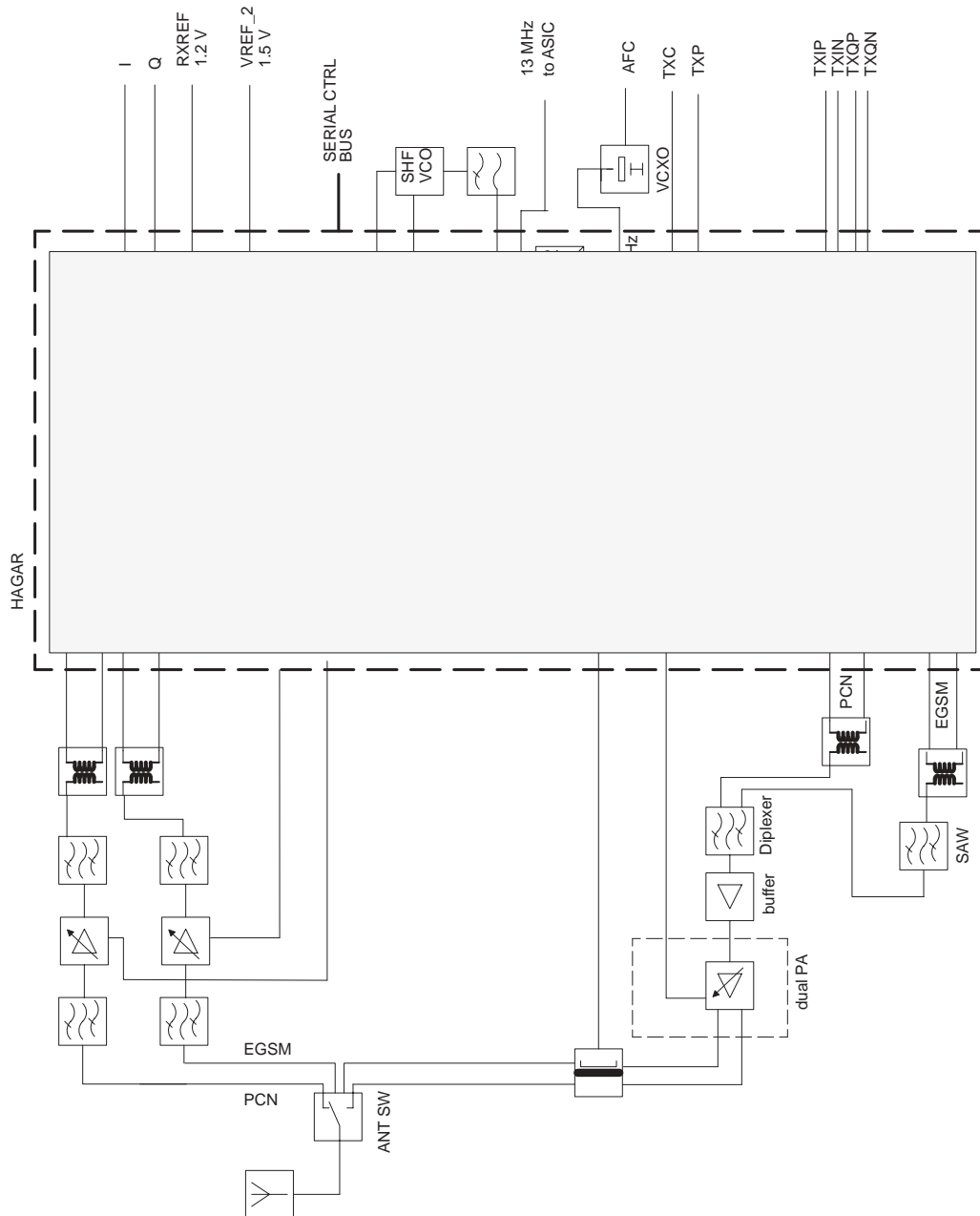
> VREF_2 from CCONT IC and RXREF from COBBA IC are used as the reference voltages for HAGAR RF-IC, VREF_2 (1.5V) for bias reference and RXREF (1.2V) for RX ADC's reference.

Power Distribution Diagram

3.9 V

BATTERY ──────────────◁ VBATT

1.76 A

PA ──────────────◁ Vpc (Hagar)

──────────────◁ VXOENA

──────────────◁ SYNPWR

| VR 1 | VR 2 | VR 3 | VR 4 | VR 5 | VR 6 | VR 7 | V5V | VREF |

vxo   vrx   vsyn_1   vsyn_2   vtx   vref_2

2 mA

VCTCXO +buff.

6 mA

LNA

20 mA

COBBA analog

4.7V Reg

HAGAR bias ref

20 mA

VCO

RX: 26 mA
TX: 29 mA   7.7 mA

RX: 18.5 mA
TX: 31.5 mA   67 mA

1.3 mA   1.6 mA

HAGAR RF–IC
RX / TX parts
PLL

──────────────◁ TXC

──────────────◁ TXP

RF Functional Description

Architecture contains one RF-IC, dualband PA module, VCO-module, VCTCXO module and discrete LNA stages for both receive bands.
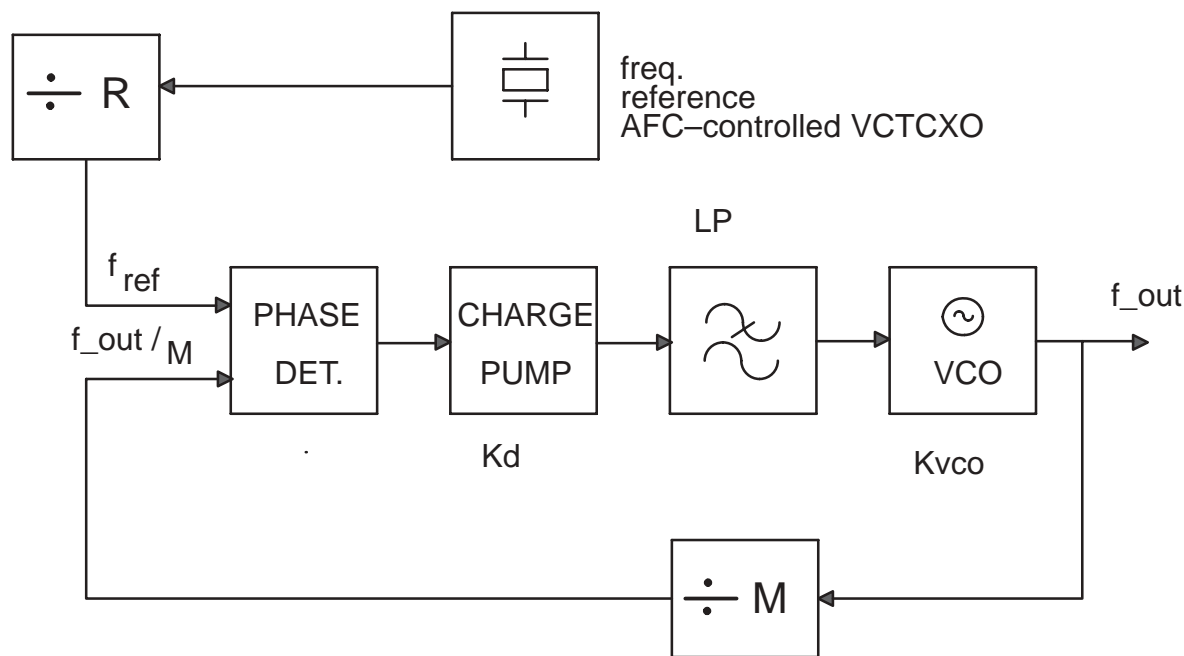

Frequency synthesizer

VCO frequency is locked with PLL into stable frequency source, which is a VCTCXO-module (voltage controlled temperature compensated crystal oscillator). VCTCXO is running at 26 MHz. Temperature effect is con trolled with AFC (automatic frequency control) voltage. VCTCXO is locked into frequency of the base station. AFC is generated by baseband with a 11 bit conventional DAC in COBBA.

PLL is located in HAGAR RF-IC and is controlled via serial bus from COBBA-IC (baseband).

Included are prescaler, N- and A-divider, reference divider, phase detector and charge pump for the external loop filter. SHF local signal, generated by a VCO-module (VCO = voltage controlled oscillator), is fed to prescaler. Prescaler is a dual modulus divider. Output of the prescaler is fed to N- and A-divider, which produce the input to phase detector. Phase detector compares this signal to reference signal (400kHz), which is divided with reference divider from VCTCXO output. Output of the phase detector is connected into charge pump, which charges or discharges integrator capacitor in the loop filter depending on the phase of the measured frequency compared to reference frequency.

Loop filter filters out the pulses and generates DC control voltage to VCO. Loop filter defines step response of the PLL (settling time) and effects to stability of the loop, that's why integrator capacitor has got a resistor for phase compensation. Other filter components are for sideband rejection. Dividers are controlled via serial bus. SDATA is for data, SCLK is serial clock for the bus and SENA1 is a latch enable, which stores new data into dividers.

LO-signal is generated by SHF VCO module. VCO has double frequency in DCS1800 and x 4 frequency in EGSM compared to actual RF channel frequency. LO signal is divided by two or four in HAGAR (depending on system mode).

Receiver

Receiver is a direct conversion, dualband linear receiver. Received RF-signal from the antenna is fed via RF-antenna switch to 1st RX dualband SAW filter and discrete LNAs (low noise amplifier), separate LNA branches for EGSM900 and DCS1800. Gain selection control of LNAs comes from HAGAR IC. Gain step is activated when RF-level in antenna is about -43 dBm.

After the LNA amplified signal (with low noise level) is fed to bandpass filter (2nd RX

dualband SAW filter). RX bandpass filters defines how good are the blocking characteristics against spurious signals outside receive band and the protection against spurious responses.

These bandpass filtered signals are then balanced with baluns. Differential RX signal is amplified and mixed directly down to BB frequency in HA GAR. Local signal is generated with external VCO. VCO signal is divided by 2 (DCS1800) or by 4 (EGSM900). PLL and dividers are in HAGAR-IC.

From the mixer output to ADC input RX signal is divided into I- and Q-signals. Accurate phasing is generated in LO dividers. After the mixer DTOS amplifiers convert the differential signals to single ended. DTOS has two gain stages. The first one has constant gain of 12dB and 85kHz cut off frequency. The gain of second stage is controlled with control signal g10. If g10 is high (1) the gain is 6dB and if g10 is low (0) the gain of the stage is –4dB.

The active channel filters in HAGAR provides selectivity for channels (–3dB @ +/-100 kHz typ.). Integrated base band filter is active-RC-filter with two off-chip capacitors. Large RC-time constants needed in the channel select filter of direct conversion receiver are produced with large off-chip capacitors because the impedance levels could not be increased due to the noise specifications. Baseband filter consists of two stages, DTOS and BIQUAD. DTOS is differential to single-ended converter having 8dB or 18dB gain. BIQUAD is modified Sallen-Key Biquad.

Integrated resistors and capacitors are tunable. These are controlled with a digital control word. The correct control words that compensate for the process variations of integrated resistors and capacitors and of tolerance of off chip capacitors are found with the calibration circuit.

Next stage in the receiver chain is AGC-amplifier, also integrated into HA GAR. AGC has digital gain control via serial mode bus from COBBA IC. AGC-stage provides gain control range (40 dB, 10 dB steps) for the receiver and also the necessary DC compensation. One 10 dB AGC step is implemented in DTOS stages.

DC compensation is made during DCN1 and DCN2 operations (controlled via serial bus). DCN1 is carried out by charging the large external capacitors in AGC stages to a voltage which cause a zero dc-offset. DCN2 set the signal offset to constant value (RXREF 1.2 V). The RXREF signal (from COBBA GJP) is used as a zero level to RX ADCs.

Single ended filtered I/Q-signal is then fed to ADCs in COBBA-IC. Input level for ADC is 1.4 Vpp max.

Transmitter

Transmitter chain consists of final frequency IQ-modulator, dualband power amplifier and a power control loop.

I- and Q-signals are generated by baseband also in COBBA-ASIC. After post filtering (RC-network) they go into IQ-modulator in HAGAR. LO-signal for modulator is generated by

VCO and is divided by 2 or by 4 de pending on system mode, EGSM/DCS1800. After mod-
ulator the TX-signal is amplified and buffered. There are separate outputs for both EGSM
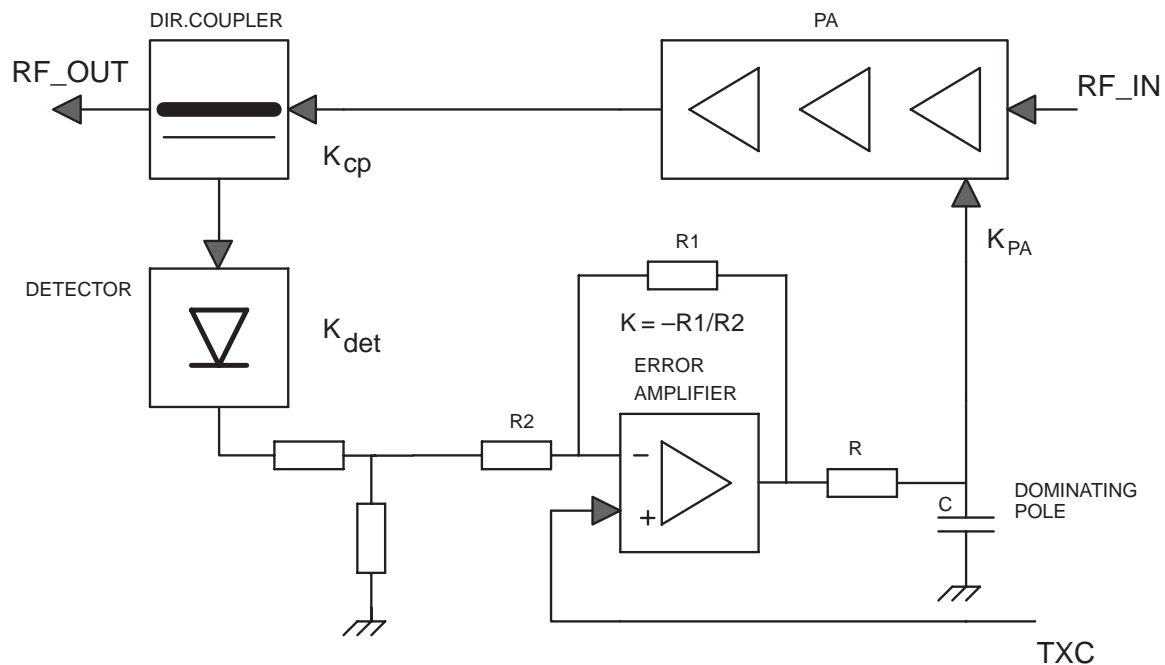and DCS1800. HAGAR TX output level is 5 dBm minimum.

Next TX signals are converted to single ended by discrete baluns. EGSM and DCS1800
branches are combined at a diplexer. In EGSM branch there is a SAW filter before
diplexer to attenuate unwanted signals and wideband noise from the Hagar IC.

The final amplication is realized with dualband power amplifier. It has one 50 ohm input
and two 50 ohm outputs. There is also a gain control, which is controlled with a power
control loop in HAGAR. PA is able to produce over 2 W (3 dBm input level) in EGSM band
and over 1 W (6 dBm input level) in DCS1800 band into 50 ohm output. Gain control
range is over 35 dB to get desired power levels and power ramping up and down.

Power control circuitry consists of discrete power detector (common for EGSM and
DCS1800) and error amplifier in HAGAR. There is a direction al coupler connected
between PA output and antenna switch. It is a dual band type and has input and outputs
for both systems. Dir. coupler takes a sample from the forward going power with certain
ratio. This signal is rectified in a schottky-diode and it produces a DC-signal after filter-
ing.

This detected voltage is compared in the error-amplifier in HAGAR to TXC-voltage, which
is generated by DA-converter in COBBA. TXC has got a raised cosine form ($\cos^4$ - func-
tion), which reduces switching transients, when pulsing power up and down. Because
dynamic range of the detector is not wide enough to control the power (actually RF out-
put volt age) over the whole range, there is a control named TXP to work under detected
levels. Burst is enabled and set to rise with TXP until the output level is high enough, that
feedback loop works. Loop controls the output via the control pin in PA to the desired
output level and burst has got the waveform of TXC-ramps. Because feedback loops
could be unstable, this loop is compensated with a dominating pole. This pole decreases
gain on higher frequencies to get phase margins high enough. Power control loop in

HAGAR has two outputs, one for both freq. bands.

AGC strategy

AGC-amplifier is used to maintain output level of the receiver in certain range. AGC has to be set before each received burst, this is called pre-monitoring.

There is 50 dB accurate gain control (10 dB steps) and one larger step (~30 dB) in LNA. LNA AGC step size depends on channel with some amount.

RSSI must be measured accurately on range -48...-110 dBm. After -48 dBm level MS reports to base station the same reading.

Production calibration is done with two RF-levels, LNA gain step is not calibrated.

AFC function

AFC is used to lock the transceivers clock to frequency of the base station. AFC-voltage is generated in COBBA with 11 bit DA-converter. There is a RC-filter in AFC control line to reduce the noise from the converter. Settling time requirement for the RC-network comes from signal ling, how often PSW (pure sine wave) slots occur. They are repeated after 10 frames, meaning that there is PSW in every 46 ms. AFC tracks base station frequency continuously, so transceiver has got a stable frequency, because changes in VCTCXO-output don't occur so fast (temperature).

Settling time requirement comes also from the start up-time allowed. When transceiver is in sleep mode and "wakes" up to receive mode, there is only about 5 ms for the AFC-voltage to settle. When the first burst comes in system clock has to be settled into +/- 0.1 ppm frequency accuracy. The VCTCXO-module requires also 5 ms to settle into final frequency. Amplitude rises into full swing in 1...2 ms, but frequency settling time is higher so this oscillator must be powered up early enough.

DC–compensation

DC compensation is made during DCN1 and DCN2 operations (controlled via serial bus). DCN1 is carried out by charging the large external capacitors in AGC stages to a voltage which cause a zero dc-offset. DCN2 set the signal offset to constant value (RXREF 1.2 V).

Receiver characteristics

Item	Values
Type	Direct conversion, Linear, DualBand, FDMA/TDMA
LO frequencies	3700... 3840 MHz / 3610... 3760 MHz
Typical 3 dB bandwidth	+/- 104 kHz
Sensitivity	min. - 102 / - 102 dBm (EGSM/PCN), S/N >8 dB
Total typical receiver voltage gain (from antenna to RX ADC)	90 dB
Receiver output level (RF level -95 dBm)	350 mVpp, single ended I/Q-signals to RX ADCs
Typical AGC dynamic range	80 dB
Accurate AGC control range	50 dB
Typical AGC step in LNA	30 dB
Usable input dynamic range	-102... -10 dBm
RSSI dynamic range	-110... -48 dBm
Compensated gain variation in receiving band	+/- 1.0 dB

Transmitter characteristics

Item	Values
Type	Direct conversion, dualband, non-linear, FDMA/TDMA
LO frequency range	3520... 3660 / 3420... 3570 MHz
Output power	2 W / 1 W peak
Gain control range	min. 30 dB
Maximum phase error (RMS/peak)	max 5 deg./20 deg. peak

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